REMARKS

Claims 1, 11, 18, 24, 34, and 39 been amended. The amendments are supported in the specification on page 20, line 19 through page 21, line 8, among other places. Claims 1-47 remain pending.

The Examiner rejected claims 1, 3-9, 18, 19, 22-25, 27-30, 34, 37-39, and 41-44 under 35 U.S.C. §103(a) as being unpatentable over Forslund (U.S. patent 5,659,630) in view of Panofsky (U.S. patent 4,445,137). The Examiner has also rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over Forslund and Panofsky in view of Garza et al. (US 6,081,659). Claims 11-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Forslund and Panofsky in view of Pial et al. (US 5,357,632). Additionally, claims 20 and 35 are rejected under 35 U.S.C. §103(a) as being unpatentable over Forslund, Panofsky, and Kober (4,181,936). Claims 21, 26, 36, and 40 are rejected under 35 U.S.C. §103(a) as being unpatentable over Forslund, Panofsky, and Schmuter (4,999,785). Claims 31-33 and 45-47 are rejected under 35 U.S.C. §103(a) as being unpatentable over Forslund, Panofsky, and McCubbrey (4,484,394). The Examiner's rejections are respectfully traversed as follows.

Claim 1 is generally directed towards an "apparatus for analyzing a plurality of image portions of at least a region of a sample." Claim 1 also requires "a plurality of processors arranged to receive and analyze at least one of the image portions" where "the processors [are] arranged to operate in parallel and [are] dynamically configurable to implement one or more algorithms from a plurality of different algorithms for analyzing the image portions selected to determine whether the corresponding regions of the sample are defective." Claim 1 also requires "a data distribution system arranged to receive image data, select at least a first processor for receiving a first image portion of the image data and one or more first algorithms selected from the plurality of different algorithms, select at least a second processor for receiving a second image portion of the image data and one or more second algorithms selected from the plurality of different algorithms, output the first image portion to the first processor and the second image portion to the second selected processor, and dynamically configure the first processor with the one or more first algorithms and the second processor with the one or more selected algorithms." In other words, the present invention includes parallel processors which are each dynamically configurable with one or more algorithms selected from different algorithms. These and the use of such features provide great flexibility in the processing of images to determine whether corresponding samples are defective. For example, two different images may be differently processed "on the fly" in parallel by two different processors configured with two different algorithm sets to determine whether the sample is defective.

Independent claim 11 is directed towards an "apparatus for inspecting a plurality of image portions of at least a region of a sample." Claim 11 requires "a plurality of distributors arranged to receive the image portions" and "a plurality of processors that are arranged into a plurality of subgroups that are each coupled to an associated distributor." Claim 11 also require that "each processor [is] dynamically configurable to implement one or more algorithms selected from a plurality of different algorithms for analyzing the image portions to determine whether the corresponding regions of the sample are defective, each distributor [is] configurable to dynamically select one or more algorithms selected from the plurality of different algorithms, output selected image portions to its associated subgroup of processors, and dynamically configure its associated processor with its selected one or more algorithms, at least two of the processors [are] arranged to analyze at least two of the image portions in parallel."

Independent claim 18 is directed towards a method and requires "receiving data derived from the inspection in a multiprocessor system" and "the system comprising a master processor and a plurality of slave processors," where "each slave processor is dynamically configurable to implement one or more algorithms selected from a plurality of different algorithms to determine whether the corresponding portions of the sample are defective." Claim 18 also recites "selecting one or more algorithms from the plurality of different algorithms for each slave processor and configuring each slave processor with the selected one or more algorithms for such each slave processor" and then "processing the data groups with the slave processors based on the selected one or more algorithms for each slave processor." Claim 24 is also a method claim and requires "outputting each image portion to a selected processor, at least some of the image portions going to different processors" where "each being dynamically configurable to implement one or more algorithms selected from a plurality of different algorithms for analyzing the image portions to determine whether the corresponding portions of the sample are defective." Claim 24 also requires "selecting one or more algorithms from the different algorithms of each selected processor and configuring each selected processor with its selected one or more algorithms." Claim 24 also requires "analyzing each image portion for defects within the selected processor based on the selected one or more algorithms for such selected processor." Claims 34 and 39 are directed towards computer readable medium and have limitations similar to method claims 18 and 24, respectively.

In contrast, the primary reference Forslund discloses a fixed system for processing images using fixed hardware. Specifically, Forslund discloses fixed parallel circuits or "channels." Each channel circuit is designed to process a different type of defect, such as shorts or opens. In Figure 5, Forslund refers to these channels as "defect detection channels hardware." (Emphasis added). Also see Figures 12 and 18 which illustrate fixed hard-wired implementations of the short and open defect circuits, respectively.

Although Forslund does suggest that these channels can be modified in column 13, lines 40-43, modification of a hardware channel would necessarily require significant time and expense to replace the actual circuits and then test the new circuitry, in contrast to processors which are each dynamically configurable or modifiable "on the fly" to implement one or more algorithms selected from a plurality of different algorithms. Additionally, Forslund merely teaches that "[w]hen new and different product parts pose new defect specifications, additional channels can be added or current ones can be modified...An example of a channel modification might be to render opens defects on different widths of land patterns." Given the nature of the hardware aspect of the channels, modification would imply a hardware modification. This passage in no way suggests modification of a channel so as to result in a channel that is dynamically configurable to implement one or more algorithms selectable from a plurality of different algorithms, in the manner claimed. In other words, even after modification each channel is capable of implementing only a single fixed algorithm, and is not dynamically configurable with a plurality of different algorithms. The modification of a channel does not result in a channel which is capable of being dynamically configured with a plurality of different algorithms. Said in another way, this passage of Forslund merely teaches modifying the hardware of a channel, and the modified hardware channel is then not dynamically configurable to implement one or more algorithms selected from a plurality of different algorithms. It is also noted that this passage also does not provide motivation for modifying the channels to be dynamically configurable to implement one or more algorithms selected from a plurality of different algorithms.

In sum, Forslund fails to teach or suggest parallel processors which are *each dynamically configurable* with *different* algorithms to implement one or more algorithms selected from a plurality of different algorithms, in the manner claimed. Accordingly, Forslund necessarily also fails to teach or suggest a mechanism for *dynamically configuring* such parallel processors to implement one or more algorithms *selected from a plurality of different algorithms*, in the manner claimed. Since the channels of Forslund are fixed circuits, Forslund necessarily fails to teach or suggest a mechanism for dynamically configuring a channel with one or more algorithms selected from a plurality of different algorithms in the manner claimed.

Although the secondary reference Panofsky does teach image processors which modify images and these processors are configurable, the feature of configurable image processors cannot be combined with the teaching of Forslund. If one were to replace the channels of Forslund with dynamically configurable processors, the combination would not operate correctly. The combination would still lack a mechanism for dynamically configuring a now

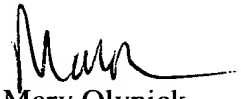
dynamically configurable channel to implement one or more algorithms selected from a plurality of different algorithms.

For the forgoing reasons, it is submitted that claims 1, 11, 18, 24, 34, and 39 are patentable over the cited references.

The Examiner's rejections of the dependent claims are also respectfully traversed. However, to expedite prosecution, all of these claims will not be argued separately. Claims 2-10, 12-17, 19-23, 25-33, 35-38, and 40-47 each depend directly from independent claims 1, 11, 18, 24, 34, or 39 and, therefore, are respectfully submitted to be patentable over cited art for at least the reasons set forth above with respect to claims 1, 11, 18, 24, 34, and 39. Further, the dependent claims require additional elements that when considered in context of the claimed inventions further patentably distinguish the invention from the cited art.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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